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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GANDHI, DIPAKKUMAR B	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/939,743	LAGOON ET AL.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,10 and 17-23* is/are rejected.

7)☒ Claim(s) *6-9 and 11-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/23/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because in figure 1, test engine is labeled as "23", but in specification page 11 line 10, test engine is labeled as "16". The test engine in figure 1 should be labeled as "16". Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The attempt to incorporate subject matter into this application by reference to U.S. Patent Application No. 09/020,792 filed on February 6, 1998 is improper because the U.S. patent number 6182258 corresponding to this application is already issued on 1/30/2001. The reference should be made to the patent issued.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1, 2, 3, 10, 17, 20, 21, 22, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barrett (US 6,134,512) in view of Johnson (US 2002/0019975 A1) and Zimmermann et al. (US 2002/0055807 A1).

As per claim 1, Barrett teaches a method for providing a bitwise constraint for test generation (col. 1, lines 25-30, lines 44-52, col. 5, lines 23-24, Barrett).

However Barrett does not explicitly teach the specific use of the method comprising: providing a language structure for expressing the bitwise constraint, said language structure including at least one constraint parameter and at least one operator.

Johnson in an analogous art teaches to extend and define the concept of a binary bit number (1/0 or T/F) to a probability bit vector (bittor) allowing for a continuous range of probabilities of truth (page 2, paragraph 16, Johnson). Extend and define the concept of propositional calculus of AND, NOT, OR, Equivalence, Implication, etc. to a new algebraic structure (a bittor algebra), page 2, paragraph 17, Johnson. Extend the formalism of algorithmic structures for computers to a multithreaded computation (page 2, paragraph 21, Johnson). Extend and define the uses of all of these structures to real world applications as embodied in computational machines of any type (whether they be mechanical, electrical, optical, or mixtures of these with other physical, chemical, and biological embodiments) that are designed from the structures disclosed herein (page 2, paragraph 22, Johnson). Johnson also teaches that for "one" or "truth" and x.sub.0 is the probability to be "0" or "false" with the requirement that both x.sub.1 and x.sub.0 be non-negative real numbers with the constraint x.sub.1+x.sub.0=1 (page 3, paragraph 33, Johnson).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Barrett's patent with the teachings of Johnson by including an additional step of the method comprising: providing a language structure for expressing the bitwise constraint, said language structure including at least one constraint parameter and at least one operator.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to generate test data to verify the design for a device in different test conditions.

Barrett also does not explicitly teach the specific use of the constraint parameter being further constrained to an interval containing at least one value, said interval having interval limits; propagating information bi-directionally to determine interval limits for said constraint parameters at least partially according to the bitwise constraint; and computing one or more permissible values for the constraint parameter.

However Zimmermann et al. in an analogous art teach that for example, a plausibility check may consist of or include a verification that a selected value lies within a given band of permissible values. Preferably, the band is defined by interval limits that are stored in memory and are of a magnitude which assures, in the case of adaptive parameters, that the adaptions performed by the control device during the operation of the vehicle will not cause the respective parameter value to fall out of the check interval (page 6, paragraph 102, Zimmermann et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Barrett's patent with the teachings of Zimmermann et al. by including an additional step of using the constraint parameter being further constrained to an interval containing at least one value, said interval having interval limits; propagating information bi-directionally to determine interval limits for said constraint parameters at least partially according to the bitwise constraint; and computing one or more permissible values for the constraint parameter.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to generate accurate values of the constraint parameters and the interval for generating test data to verify the design for the device.

- As per claim 2, Barrett, Johnson and Zimmermann et al. teach the additional limitations.

Barrett teaches the method further comprising: generating a single test value for the constraint parameter (figure 2, col. 2, lines 62-64, Barrett).

- As per claim 3, Barrett, Johnson and Zimmermann et al. teach the additional limitations.

Johnson teaches that the interval is representable as a bitwise representation (page 2, paragraph 16, Johnson). Zimmermann et al. teach that interval is representable as an arithmetic range (page 9, paragraph 165, Zimmermann et al.).

- As per claim 10, Barrett, Johnson and Zimmermann et al. teach the additional limitations.

Barrett teaches that the bitwise constraint is derived from a constraint featuring an operator through propagation of bitwise information (col. 3, lines 30-40, Barrett).

- As per claim 17, Barrett, Johnson and Zimmermann et al. teach the additional limitations.

Barrett teaches a method for providing a bitwise constraint for test generation (col. 1, lines 25-30, lines 44-52, col. 5, lines 23-24, Barrett).

Johnson teaches providing a language structure for expressing the bitwise constraint, said language structure including one or more constraint parameters and at least one operator (page 2, paragraphs 16, 17, 21, 22, page 3, paragraph 33, Johnson).

Zimmermann et al. teach constraint parameter having a range list containing at least one value; propagating information bi-directionally to determine limits for said constraint parameters; and generating a test value for the bitwise constraint (page 6, paragraph 102, Zimmermann et al.).

- As per claim 20, Barrett, Johnson and Zimmermann et al. teach the additional limitations.

Barrett teaches a method of test generation using a bitwise constraint and applying the bitwise constraint to the bitwise representation to perform the test generation (col. 1, lines 25-30, lines 44-52, col. 5, lines 23-24, Barrett).

Johnson teaches a range list having a bitwise constraint (page 2, paragraph 16, Johnson).

Johnson teaches providing a computational structure for containing the range list and a bitwise representation of the range list; translating the range list to provide said bitwise representation of the range list (page 2, paragraphs 16-17, Johnson).

Zimmermann et al. teach a range list having an arithmetic constraint and applying the arithmetic constraint to the range list to perform the test generation (page 6, paragraph 102, page 9, paragraph 165, Zimmermann et al.).

- As per claim 21, Barrett, Johnson and Zimmermann et al. teach the additional limitations.

Johnson teaches performing a union (page 8, paragraph 82, page 9, paragraph 84, Johnson). Johnson teaches a plurality of range lists and of a plurality of said bitwise representations of a plurality of range lists (page 2, paragraph 16, Johnson).

Barrett teaches resolving bitwise constraints (col. 1, lines 25-30, lines 44-52, col. 4, lines 62-67, col. 5, lines 1-2, Barrett).

Zimmermann et al. teach arithmetic constraints (page 6, paragraph 102, page 9, paragraph 165, Zimmermann et al.).

- As per claim 22, Barrett, Johnson and Zimmermann et al. teach the additional limitations.

Johnson teaches a method for bitwise representation of a range list and translating the range list to provide the bitwise representation of the range list (page 2, paragraph 16, Johnson).

Zimmermann et al. teach a range list having an arithmetic constraint (page 9, paragraph 165, Zimmermann et al.).

Barrett teaches a bitwise constraint (col. 1, lines 41-52, Barrett) and propagating the arithmetic constraint and the bitwise constraint to determine at least one new range according to both the arithmetic constraint and the bitwise constraint (col. 4, lines 66-67, col. 5, lines 1-2, Barrett) and computing one or more permissible values for the constraint parameter (col. 3, lines 30-40, Barrett).

- As per claim 23, Barrett, Johnson and Zimmermann et al. teach the additional limitations.

Barrett teaches generating a value (col. 2, lines 62-64, Barrett) according to the at least one new range (col. 4, lines 66-67, col. 5, lines 1-2, Barrett).

6. Claims 4, 5, 18, 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barrett (US 6,134,512), Johnson (US 2002/0019975 A1) and Zimmermann et al. (US 2002/0055807 A1) as applied to claim 3 above, and further in view of Takeshita (JP 02154530 A).

As per claim 4, Barrett, Johnson and Zimmermann et al. substantially teach the claimed invention described in claim 3 (as rejected above).

Johnson also teaches providing the language structure that comprises providing a computational structure (page 2, paragraph 17, Johnson). Zimmermann et al. teach representing the interval as the arithmetic range and interval limits (page 9, paragraph 165, Zimmermann et al.).

However Barrett, Johnson and Zimmermann et al. do not explicitly teach the specific use of representing the arithmetic range and the bitwise representation in parallel and for propagating information.

Takeshita in an analogous art teaches that to attain high speed conversion into a binary number even with a decimal number of a large digit number by applying n/i ((n) is number of digits of a decimal number and (i) is a number of digits of a binary number) times of parallel processing (abstract, Takeshita).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Barrett's patent with the teachings of Takeshita by including an additional step of representing the arithmetic range and the bitwise representation in parallel and for propagating information.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to convert test data range from decimal to binary format for testing the design of a device.

- As per claim 5, Barrett, Johnson, Zimmermann et al. and Takeshita teach the additional limitations.

Johnson teaches that the language structure comprises a plurality of constraint parameters and wherein said computational structure is provided (page 2, paragraphs 16-22, page 3, paragraph 33, Johnson).

Barrett teaches reducing at least a portion of said plurality of constraint parameters wherein the reducing comprises computing a new set of values for a first constraint parameter and propagating the new set of values to at least one other constraint parameter (col. 4, lines 62-67, col. 1-2, Barrett).

- As per claim 18, Barrett, Johnson, Zimmermann et al. and Takeshita teach the additional limitations.

Barrett teaches a method for providing a bitwise constraint (col. 1, lines 25-30, lines 44-52, col. 5, lines 23-24, Barrett) and generating a test value for the bitwise constraint (figure 2, col. 2, lines 62-64, Barrett).
Zimmermann et al. teach a range list constraint for test generation with an arithmetic range list, the arithmetic range list containing at least one arithmetic value and propagating information bi-directionally to determine limits for said constraint parameters (page 6, paragraph 102, Zimmermann et al.).
Johnson teaches providing a language structure including one or more constraint parameters for the bitwise constraint and for the range list constraint and at least one operator (page 2, paragraphs 16, 17, 21, 22, page 3, paragraph 33, Johnson).
Takeshita teaches expressing the bitwise constraint with regard to the arithmetic list in parallel to the range list constraint (abstract, Takeshita).

- As per claim 19, Barrett, Johnson, Zimmermann et al. and Takeshita teach the additional limitations.

Johnson teaches a method for bitwise representation of a range list (page 2, paragraph 16, Johnson).
Zimmermann et al. teach a range list having an arithmetic constraint (page 9, paragraph 165, Zimmermann et al.).
Barrett teaches a bitwise constraint (col. 1, lines 25-30, lines 44-52, col. 5, lines 23-24, Barrett).
Johnson teaches translating the range list to a bitwise list (page 2, paragraph 16, Johnson).
Takeshita teaches solving the arithmetic constraint together with the bitwise list constraint while using one or both of the range list and said bitwise list (abstract, Takeshita).

Allowable Subject Matter

7. Claims 6 to 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an Examiner's statement of reasons for the indication of allowable subject matter:
The present invention pertains to a method for enabling bitwise or bit slice constraints to be provided as part of test generation process, by providing a language structure, which enables these constraints to be expressed in a test generation language. Claim 6 recites various features: "computational structure

comprises a range list representation which includes an arithmetic range and a bitwise representation, wherein reducing at least a portion of said plurality of constraint parameters is performed by: computing a first range in a first range list for at least a first constraint parameter; computing one or more ranges in a second range list for at least a second constraint parameter; and intersecting said first range list with said second range list to reduce said first and second constraint parameters."

The prior art of record teach means for providing input bits that comprises means for providing unconstrained bits and means for constraining the unconstrained bits whereby the set of constraints is satisfied (Barrett US 6,134,512 is an example of such prior arts). The prior arts, however, do not teach that reducing at least a portion of said plurality of constraint parameters is performed by: computing a first range in a first range list for at least a first constraint parameter; computing one or more ranges in a second range list for at least a second constraint parameter; and intersecting said first range list with said second range list to reduce said first and second constraint parameters. Hence the prior arts of record taken alone or in any combination fail to teach the novel feature in claim 6 in view of its base and intervening claims. Claims 7-9 are dependent claims on claim 6, hence the prior arts of record taken alone or in any combination fail to teach the novel feature in claims 7-9.

8. Claims 11 to 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The present invention pertains to a method for enabling bitwise or bit slice constraints to be provided as part of test generation process, by providing a language structure, which enables these constraints to be expressed in a test generation language. Claim 11 recites various features: "bi-directional propagation is at least partially performed by indicating bits having one or zero value according to a maximum of said interval."

The prior art of record teach means for providing input bits that comprises means for providing unconstrained bits and means for constraining the unconstrained bits whereby the set of constraints is satisfied (Barrett US 6,134,512 is an example of such prior arts). The prior arts, however, do not teach

that bi-directional propagation is at least partially performed by indicating bits having one or zero value according to a maximum of said interval. Hence the prior arts of record taken alone or in any combination fail to teach the novel feature in claim 11 in view of its base and intervening claims. Claims 12 to 16 are dependent claims on claim 11, hence the prior arts of record taken alone or in any combination fail to teach the novel feature in claims 12 to 16.

Claim Rejections - 35 USC § 101

9. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1 to 23 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims 1 to 23 should include "computer generated method for test generation" and "computer programming language".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 703-305-7853. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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